

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:
a clock non-synchronous type circuit for
performing data read operation on the basis of a read
control signal and outputting read data from a data
5 output node asynchronously with a clock signal;

a clock synchronous type circuit for receiving the
read data through a data input node in synchronism with
the clock signal;

10 data storage circuits connected in parallel
between the data output node and the data input node;

a first transfer timing determining circuit for
selecting one of said data storage circuits and
transferring the read data output from said clock
non-synchronous type circuit to said selected one data
15 storage circuit, said first transfer timing determining
circuit transferring the read data on the basis of a
first control signal representing that the read data is
output from said clock non-synchronous type circuit;

20 and

a second transfer timing determining circuit for
selecting one of said data storage circuits and
transferring the read data stored in said selected one
data storage circuit to said clock synchronous type
25 circuit, said second transfer timing determining
circuit transferring the read data on the basis of a
second control signal synchronous with the clock signal.

09966667-099704
T02260/2999660

2. A circuit according to claim 1, wherein each of said data storage circuits comprises a latch circuit for latching the read data, a first switching circuit connected between the data output node and said latch circuit, and a second switching circuit connected between the said latch circuit and the data input node.

3. A circuit according to claim 2, wherein said first transfer timing determining circuit controls said switching circuit, and said second transfer timing determining circuit controls said second switching circuit.

4. A circuit according to claim 1, wherein each of said data storage circuits comprises first and second latch circuits having a switching function and connected in series between the data output node and the data input node.

5. A circuit according to claim 4, wherein said first transfer timing determining circuit controls said first latch circuit, and said second transfer timing determining circuit controls said second latch circuit.

6. A circuit according to claim 1, wherein each of said data storage circuits comprises first and second flip-flop circuits connected in series between the data output node and the data input node.

7. A circuit according to claim 6, wherein said first transfer timing determining circuit controls said first flip-flop circuit, and said second transfer

timing determining circuit controls said second
flip-flop circuit.

8. A circuit according to claim 1, wherein the
first control signal is output from said clock
5 non-synchronous type circuit and asynchronous with the
clock signal.

9. A circuit according to claim 1, wherein the
first control signal is generated on the basis of the
read control signal, and is output from said clock
10 non-synchronous type circuit after a lapse of a delay
time corresponding to a time interval between the
instant at which the data read operation is started and
the instant at which the read data is output from said
clock non-synchronous type circuit.

10. A circuit according to claim 1, wherein the
second control signal determines a timing of transfer
of the read data to said clock synchronous type circuit
on the basis of the read control signal.

11. A circuit according to claim 1, wherein said
20 clock non-synchronous type circuit has a function of a
DRAM which operates asynchronously with the clock
signal.

12. A semiconductor integrated circuit comprising:
a clock non-synchronous type circuit for
25 performing data read operation on the basis of a read
control signal and outputting read data from a data
output node asynchronously with a clock signal;

0996567-092701

```

        a selection circuit;
5         first data storage circuits connected in parallel
        between the data output node and said selection
        circuit;

```

10 a first transfer timing determining circuit for
selecting one of said first data storage circuits and
transferring the read data output from said clock
non-synchronous type circuit to said selected one first
data storage circuit, said first transfer timing
15 determining circuit transferring the read data on the
basis of a first control signal representing that the
read data is output from said clock non-synchronous
type circuit; and

13. A circuit according to claim 12, wherein said selection circuit has a function of transferring the

of the read data to said clock synchronous type circuit on the basis of the read control signal.

20. A circuit according to claim 12, wherein said clock non-synchronous type circuit has a function of a
5 DRAM which operates asynchronously with the clock signal.

09/09/2009 10:22:04